FRAUNHOFER INSTITUTE FOR PHOTONIC MICROSYSTEMS IPMS

PRESS RELEASE

RISC-V Functional Safety Processor IP Core introduced by Fraunhofer IPMS and CAST

The Fraunhofer Institute for Photonic Microsystems IPMS and semiconductor intellectual property provider CAST, Inc. announced the immediate availability of EMSA5-FS, a fault-tolerant embedded RISC-V processor IP core designed to meet the most stringent functional safety requirements of automotive, airborne, and other safety-critical applications.

Developed by Fraunhofer IPMS, the EMSA5-FS Embedded Functional Safety RISC-V Processor is a 32-bit, in-order, single-issue, five-stage pipeline processor supporting the open standard RISC-V instruction set architecture (ISA). Its fail-safe features include built-in triple or double modular redundancy (with lockstep), error correction code (ECC) protection of buses, a configurable memory protection unit, privileged operation modes, and Reset and Safety Manager Modules. It is available for ASICs or FPGAs, and as either a stand-alone processor or pre-integrated in optional subsystems combining a bus fabric with typical peripherals.

With the EMSA5-FS processor's fault-tolerant design and included safety documents, users can readily achieve ISO 26262 certification up to ASIL-D, the highest Automotive Safety Integrity Level. The delivered documents include the essential FMEDA (Failure Modes, Effects, and Diagnostic Analysis), SAM (Safety Manual), and others. Available FPGA board development kits and sample designs further facilitate certification, evaluation, or rapid prototyping.

"CAST customers using our popular CAN and TSN automotive IP core have been disappointed in finding limited options for a suitable ISO 26262 compliant microcontroller core," said Nikos Zervas, CAST's chief executive officer. "The new EMSA5-FS Processor satisfies their needs and more, making the whole RISC-V ecosystem and development community available to accelerate projects while also complying with the functional safety requirements of their systems."
"We are proud to be first to market with a RISC-V ISO 26262 certifiable processor core," said Marcus Pietzsch, group manager for IP cores and ASICs at Fraunhofer IPMS. "Unlike the vast majority of processor applications, systems requiring ASIL-D are usually life-critical, and we have been diligent in engineering the EMSA5 Processor to meet that level of responsibility while also being easy for customers to integrate and program."

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Designers using the EMSA5-FS Processor can exploit any open-source and commercial RISC-V development aids, test tools, and libraries, including the GNU toolchain and the comprehensive Eclipse IDE with OpenOCD debug support. Fraunhofer is also working with third-party compiler and software tool suppliers to enable support for EMSA5-FS by commercial safety-ready development toolsets, further simplifying the path to safety certification for end-product developers.

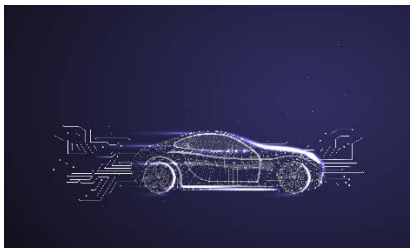
About Fraunhofer IPMS

The Fraunhofer Institute for Photonic Microsystems IPMS stands for applied research and development in the fields of intelligent industrial solutions, medical technology and improved quality of life. Our research focuses on miniaturized sensors and actuators, integrated circuits, wireless and wired data communication, and customized MEMS systems. Fraunhofer IPMS has years of experience in designing and developing IP cores for automotive communication and offers different IP cores for LIN, CAN2.0/FD/XL and Ethernet TSN. It has more than 150 IP core users worldwide - a majority of them in the automotive, aerospace and manufacturing industries. The multidisciplinary IP design team at Fraunhofer IPMS have expertise in domain-specific computer architectures, network structures over RTL design, and the implementation of electronic systems. It is also available as a competent development partner for application-specific adaptations of the IP cores as well as their integration into complex system architectures.

About CAST Inc.

CAST, Inc. develops and distributes digital IP cores for ASICs and FPGAs. The product line includes compression algorithms, microcontrollers and processors, SoC security modules as well as various peripherals, interfaces and other IP cores.

Images



Functional safety in the smart car

Marcus Pietzsch, Fraunhofer IPMS

Nikos Zervas, CAST Inc.